國立中正大學
114學年度碩士班招生考試
試 題

［第4節］

科目名稱	計算機系統
系所組別	資訊工程學系-甲組

I. 單一選擇題：每題 5 分。

1. Which of the following is wrong?

   A. Performance is best determined by running a real application.

   B. The best measurement of performance is execution time.

   C. A CPU with higher clock rate has a better performance.

   D. The best measurement of performance for a program is the product of clock cycles and cycle time.

2. Which of the following is wrong?

   A. Cache is usually implemented by SRAM.

   B. Registers are usually allocated by programmers.

   C. Virtual memory is manipulated by OS (Operating System).

   D. Main memory is usually implemented by DRAM.

3. Which the following architecture support is not helpful to code generation for compilers?

   A. More registers.

   B. Complete instruction set.

   C. Variable instructions.

   D. More addressing modes.

4. What is the primary function of a distributed file system (DFS)?

   A. Ensuring location transparency while managing files distributed across multiple nodes.

   B. Enhancing the performance of local file operations by caching remote files0.

   C. Increasing the reliability of file storage by replicating data across multiple servers.

   D. Reducing communication overhead in remote file access through network optimizations.

5. Which synchronization mechanism ensures that only one thread can access a resource at a time by blocking other threads until the resource is released?

   A. Condition variable.

   B. Semaphore with value > 1.

   C. Shared Memory.

   D. Mutex.

6. Which of the following is a key purpose of using DMA (Direct Memory Access) in I/O operations?

   A. To increase CPU utilization during I/O operations.

   B. To allow devices to directly access main memory without involving the CPU.

   C. To improve the reliability of data transfers by using checksums.

   D. To enable real-time monitoring of all data transfers.

II. 多重選擇題：所有答案必須符合才算分，每題 5 分。

1. Which of the following statements about branch prediction are true?

   A. It is helpful to solve control hazard.

   B. 2-bit branch predictor always has better performance than 1-bit branch predictor.

   C. Static branch prediction always has better performance than dynamic branch prediction.

   D. Loop unrolling is helpful to branch prediction.

2. Which of the following statements are wrong?

   A. About negative numbers, one's complement representation is better than two's complement.

   B. One's complement has only one zero.

   C. Zero-extension can be used to convert a n-bit integer into an m-bit integer, where n < m.

   D. We can use 4-bit ALU (Arithmetic Logic Unit) to build 32-bit ALU.

3. Which of the following features are typically provided by modern file systems?

   A. Journaling.

   B. File versioning.

   C. Replication across multiple nodes.

   D. Hierarchical directory structure.

4. Which of the following are benefits of using interrupts in an operating system?

   A. Minimize the latency in response to I/O events.

   B. Allow the CPU to perform other tasks while waiting for I/O operations to complete.

   C. Reduce the complexity of I/O device drivers.

   D. Support asynchronous communication between hardware and software.

III. 填空題：不需要做答過程，每個答案務必標明題號和空格編號，每個空格 5 分。

1. In memory hierarchy, the mapping unit between cache and memory is _____.

2. For a 32-bit address computer, the total bits is _____ for a direct-mapped cache with 128 K bytes of data and 4-word block size.

3. For a datapath with five pipeline stages: instruction fetch (IF), instruction decode (ID), execution (EXE), memory (MEM), and write back (WB), the following code is executed.

add	$2, $1, $3
and	$12, $2, $5
sub	$13, $6, $2
or	$14, $2, $2

   (a) Some dependency in this code segment is _____. (b) The cycles needed to execute this code is _____ without any technique. (c) We can apply _____ (*hint: technique*) to solve the hazards.

4. Consider the following set of processes with their Arrival Time, CPU burst times, I/O burst times, and two-phase CPU burst execution. Assume the CPU scheduling algorithm used is Preemptive Shortest Remaining Time First (SRTF). After completing the first CPU burst, each process performs an I/O operation before continuing with its second CPU burst. What are the waiting times for <P1, P2, P3>?

Process	Arrival Time (ms)	First CPU Burst Time (ms)	I/O Burst Time (ms)	Second CPU Burst Time (ms)
P1	0	5	4	7
P2	2	6	3	5
P3	4	8	5	6

5. A 32-bit virtual address system uses a three-level page table structure. The virtual address is divided as follows:

   First-level index: 10 bits

   Second-level index: 10 bits

   Third-level index: 6 bits

   Offset: 6 bits

   If the virtual address provided is 0x1A3F5C, and the base addresses of the page tables are as follows:

   First-level page table base: 0x1000

   Second-level page table base: 0x2000

   Third-level page table base: 0x3000

   Assume each page table entry (PTE) is 4 bytes, and the page size is 64 bytes. Calculate the address of the PTEs we need to access in each level <first-level, second-level, third-level page tables>. _____. (Please provide your answer in hexadecimal format)

6. A network server uses a semaphore to control access to a pool of database connections. Assume the maximum number of connections is 4. After 2 threads acquire a connection and another 1 thread releases a connection, the semaphore's value becomes _____.

7. Given the reference string: 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2 and 3-page frames, it will induce _____ page faults when using the Least Recently Used (LRU) page replacement algorithm.

8. In a RAID 0+1 array with 8 disks, the system can tolerate up to _____ disk failures without losing any data, provided that no entire striped set fails.